Verilog - Live Online Training Program

Introduction to VLSI Design

- Participants and Trainer Introduction
- Introduction to Digital VLSI Design
- Applications of VLSI
- Domains of VLSI
- VLSI Design Flow

Introduction to Digital Design

- Digital Signal
- Digital System
- Performance of Digital Systems over Analog Systems
- Combinational and Sequential Devices

Introduction to HDL

- Introduction to Verilog HDL
- Features of Verilog HDL
- Introduction to Different Level of Verilog Modeling

Primitive level Modeling

- Introduction to Verilog Primitives
- Primitive Modeling

Data Flow Modeling

- Introduction to Operator
- Literals
- Data Flow Modeling

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Simulation of Primitive & Data Flow Programming

- Introduction to ModelSim Software
- Working Environment at Modelsim
- Simulation of Module

Behavioral Modeling

- Introduction to Behavioral Modeling
- Control statements-if-else/case
- Designing of Digital Devices using Behavioral Modeling

Task & Function

- Introduction to Task & Function
- Creating Function in Verilog
- Creating Task in Verilog

Memory Designing

- Memory Parameters
- RAM Design : 1-port/Dual port
- ROM Design :1-port/Dual Port
- Creating Module for RAM & ROM

FSM modeling

- Steps for creating FSM Module in Verilog
- Moore & Mealy FSM designing
- Control System using FSM

File handling

- Introduction of File Handling, Role of Files in Verilog
- Creating Module for File Accessing

Switch level modeling

- Introduction to Verilog Switch
- Modeling based on Switch

Structural modeling

- Introduction to Structural Modeling
- Interfacing Methods
- Creating Top Design via Structural Modeling

Introduction to Verification

- Introduction to Verification: Functional,Timimg
- Delay
- Loops: for /while/forever/repeat/do while

Test bench

- Introduction to Test bench
- Creating Test Module
- Creating Test bench
- System Task
- Complier Directive

UDP

- Introduction & Application to UDP
- Modeling of UDP

Verilog -2001 Features

- New Port Definition
- Multiple Dimensional Array
- Generate loop, Recursive functions

Guidelines for Implementation